REMARKS/ARGUMENTS

Claims 1-3 and 5-29 are pending in this application . Claim 4 was canceled in the Preliminary Amendment filed January 6, 2004.

Rejections under 35 U.S.C. § 101

Claims 9-25 are rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants have amended claims 9-25 and respectfully request that the rejections under 35 U.S.C. § 101 be withdrawn.

Rejections under 35 U.S.C. § 102

Claims 1-3, 5-7, 9-14, 17-22, 28, and 29

Claims 1-3, 5-7, 9-14, 17-22, 28 and 29 are rejected under 35 U.S.C. § 102(b) as being anticipated by Iitsuka et al. US Patent No. 5,230,050 (hereinafter "Iitsuka"). Iitsuka generally describes a method of recompiling a program that uses the results of a previous compilation in order to reduce the time associated with recompilation. In the Office Action, Examiner cites the following sections of Iitsuka as anticipating independent claims 1, 9, 17, and 28.

> An object of the present invention is therefore to provide a compiling method which is capable of reducing the time taken for the recompilation of a program which needs to be recompiled, such as a modified procedure which requires recompilation because of the modification or an unmodified procedure requiring recompilation because of modification of other associated procedures.
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> It is another object of the present invention to provide a compiling method which is capable of reducing the portions to be recompiled in a procedure which requires recompilation.

Iitsuka at 3:15-25.

What is claimed is:

> 1. A program compiling method for transforming a first procedure included in a first source program into an object program, wherein said first source program is obtained by modifying a second source program including a second procedure corresponding to said first procedure and wherein the transformation is done by making use of a result of preceding compilation of said second procedure, said method comprising the steps, executed by an apparatus, of:
>
> (a) compiling, when said second procedure is to be compiled into a second object program, a plurality of segments obtained by splitting said second procedure into corresponding portions, wherein the compiling step includes a series of program transformation processes for compilation;

Iitsuka at 37:10-25.

Neither of the sections cited in the Office Action teach first and second instructions, that the second instruction depends on the result of the first instruction, or forming a fused instruction. The cited sections instead focus on a recompilation method that utilizes previous compilations.

Accordingly, applicants assert that Iitsuka does not anticipate independent claims 1, 9, 17, and 28, and likewise does not anticipate dependent claims 2-3, 5-7, 10-14, 16-22, and 29 for at least all the same reasons. Therefore, applicants respectfully request that the rejection of claims 1-3, 5-7, 9-14, 17-22, 28 and 29 under 35 U.S.C. § 102 be withdrawn.

Claims 23, 24, 26 and 27

Claims 23, 24, 26 and 27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Djafarian et al. US Patent No. 6,742,110 B2 (hereinafter "Djafarian"). Djafarian generally relates to a processing engine providing a verification of instruction parallelism. Independent claims 23 and 26 both recite a "a fused instruction execution

unit that includes a first arithmetic logic unit (ALU) to perform a first operation and a second ALU to perform a second operation." Examiner asserts that Djafarian teaches a fused instruction execution unit at column 2, lines 30-37, but the cited portion of Djafarian actually teaches data address generation control signal merge logic. Even assuming *arguendo* that the merge logic can be considered a fused instruction execution unit, the merge logic does not "include" what Examiner cites as the first and second ALUs, as would be required for Djafarian to anticipate claims 23 and 26.

Additionally, claims 23 and 26 recite the limitation of "wherein a result of the first ALU is input into the second ALU and within one clock cycle, the first ALU performs the first operation and the second ALU performs the second operation." Although Djafarian teaches that the D Unit can use the A Unit as a source or destination, it does not teach that the A Unit, within one clock cycle, performs a first operation and the D Unit performs a second operation, as would be required for Djafarian to anticipate claims 23 and 26.

Accordingly, applicants assert that Djafarian does not anticipate independent claims 23 and 26, and likewise does not anticipate dependent claims 24 and 27 for at least all the same reasons. Therefore, applicants respectfully request that the rejection of claims 23, 24, 26, and 27 under 35 U.S.C. § 102 be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 8, 15 and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iitsuka as applied in claims 6 and 12, in view of Djafarian. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Iitsuka as applied in claims 6 and 12, in view of Djafarian as applied in claim 24 and further in view of Odani et al. US

Patent No. 5,850,552 (hereinafter "Odani").

Claim 8 depends from independent claim 1. Claims 15 and 16 depend from independent claim 9. Claim 25 depends from independent claim 23. Accordingly, applicants submit that claims 8, 15, 16, and 25 are allowable for at least all the same reasons independent claims 1, 9, and 23 are allowable. Accordingly, applicants respectfully request that the rejections of claims 8, 15, 16, and 25 under 35 U.S.C. § 103 be withdrawn.

The Applicants respectfully submit that the present case is in condition for allowance and respectfully requests that the Examiner issue a notice of allowance.

The Office is hereby authorized to charge any fees determined to be necessary under 37 C.F.R. §1.16 or §1.17 or credit any overpayment to Kenyon & Kenyon Deposit Account No. **11-0600**.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON LLP

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/Jeffrey R. Joseph/
Jeffrey R. Joseph
(Reg. No. 54,204)
Attorneys for Intel Corporation

KENYON & KENYON LLP
333 West San Carlos St., Suite 600
San Jose, CA 95110

Telephone: (408) 975-7500
Facsimile: (408) 975-7501